a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a circuit, coupled to said word lines and said bit line, for applying a write voltage to the word line of a selected memory cell, for applying a verify voltage to the word line of the selected memory cell to determine an actual threshold voltage of the selected memory cell while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors, for applying a first level voltage to the bit line to change the threshold voltage of the selected memory cell in which it has been determined that the threshold voltage has not reached a given threshold voltage level, said first level voltage being combined with said write voltage, and for applying a second level voltage to the bit line to maintain the threshold voltage of the selected memory cell in which it has been determined that the threshold voltage has reached said given threshold voltage level, said second level voltage being combined with said write voltage;

wherein said pass voltage is higher than said verify voltage.

121. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array coupled to said bit lines and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a plurality of data latch circuits, each of said data latch circuits including plural binary data latch circuits and being coupled to a respective one of said bit lines, for storing write data in the form of combination of plural write binary data in a write operation, said write data

being written into said memory cells, and for storing reach data in the form of a combination of plural read binary data in a read operation, said read data being read from said memory cells.

123. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array coupled to said bit lines and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a data conversion circuit, coupled to a plurality of data latch circuits, for converting plurality binary input data into plural internal write binary data; and

a plurality of data latch circuits, each including plural binary data latch circuits and being coupled to a respective one of said bit lines, for storing internal write data in the form of a combination of said plural internal write binary data in a write operation, said write data being written into respective memory cells.

125. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array coupled to said bit lines and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a data conversion circuit, coupled to a plurality of data latch circuits, for converting plural internal read binary data into plural binary output data; and

a plurality of data latch circuits, each including plural binary data latch circuits and being coupled to a respective one of said bit lines, for storing internal read data in the form of a combination of said plural internal read binary data in a read operation, said read data being read from respective memory cells.

127. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array coupled to said bit lines and said word lines, said memory cell array comprising a plurality of electrically programmable memory cells, each of said memory cells having at least three storage states;

a data conversion circuit, coupled to a plurality of data latch circuits, for converting plural binary input data into plural internal write binary data, and for converting plural internal read binary data into plural binary output data; and

a plurality of data latch circuits, each including plural binary data latch circuits and being coupled to a respective one of said bit lines, for storing internal write data in the form of a combination of said plural internal write binary data in a write operation, said write data being written into respective memory cells, and for storing internal read data in the form of a combination of said plural internal read binary data in a read operation, said read data being read from respective memory cells.

A5

129. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having multi-levels storage states;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a word line selector coupled to said word lines for selecting the word line of a selected memory cell;

a data latch circuit coupled to said word lines for storing data, said data latch circuit including at least two binary data latch circuits;

a first bit line bias circuit coupled to said bit line for biasing said bit line dependent on the data stored in said data latch circuit; and

a second bit line bias circuit coupled to said bit line for biasing said bit line independent of the data stored in said data latch circuits.

A6

133. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a circuit, coupled to said word lines and said bit line, for applying one of at least two read voltages to the word line of a selected memory cell to determine whether or not a threshold voltage of the selected memory cell is higher than said one of at least two read voltages while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two read voltages.

139. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a circuit, coupled to said word lines and said bit line, for applying one of at least two verify voltages to the word line of a selected memory cell to determine whether or not a threshold voltage of the selected memory cell reaches one of said at least three threshold voltage levels while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two verify voltages.

143. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having multi-level storage states;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a word line selector coupled to said word lines for selecting the word line of a selected memory cell, the selected word line having applied thereto read voltages in a read operation, the remaining word lines of unselected memory cells in said NAND-cell unit having applied thereto a pass voltage to make unselected memory cells act as transfer transistors in said read operation, said pass voltage being higher than said read voltages; and

a bit line precharge circuit coupled to said bit line for charging said bit line at the beginning of said read operation.

150. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell; unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a circuit, coupled to said word lines and said bit line, for applying, to the word line of a selected memory cell, a first voltage in a first portion of a verify operation and a second voltage in second portion of said verify operation while applying, to remaining word lines of

unselected memory cells in said NAND-cell unit, a third voltage in said first and second portions of said verify operation.

Please add new Claims 151-174 as follows:

151. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells, each being capable of having one of first, second, and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circuits is capable of storing in a data storage portion data of one of first, second, and third logic levels which define write voltage to be applied to a corresponding memory cell, for applying said write voltage to the corresponding memory cell according to the data stored in the data storage portion, for determining whether the corresponding memory cell has reached the second storage level only in case that the data stored in the data storage portion represents the second logic level, for determining whether the corresponding memory cell has reached the third storage level only in case that the data stored in the data storage portion represents the third logic level, for modifying the stored data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored data from the third logic level to the first logic level if it has been determined that the corresponding memory cell has reached the third storage level, and for maintaining the stored data at the first logic level if the data storage portion has stored the data of the first logic level.

152. (New) The device according to claim 151, wherein the programming control circuits storing the data of the first logic level apply a first write voltage, which inhibits changes in the storage levels, to the corresponding memory cells.

Cont A10

153. (New) The device according to claim 152, wherein the programming control circuits storing the data of the second logic level apply a second write voltage, which promotes changes to the second storage level in the corresponding memory cells, to the corresponding memory cells, and the programming control circuits storing the data of the third logic level apply a third write voltage, which promotes changes to the third storage level in the corresponding memory cells, to the corresponding memory cells.

154. (New) The device according to claim 153, wherein said second write voltage is different from said third write voltage.

155. (New) The device according to claim 151, wherein each data storage portion includes two CMOS flip-flop circuits.

156. The device according to claim 151, further comprising data detectors for detecting whether all of said data storage portions have stored the data of the first logic level.

157. (New) The device according to claim 151, wherein plural of the memory cells store three-bit data.

158. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells each being capable of having one of first second and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circuits is capable of storing first data of one of first and second logic levels in a first data storage portion and capable of storing

second data of one of first and second logic levels in a second data storage portion, for applying a first write voltage to corresponding memory cell in case that the first data represents the first logic level in order to inhibit change in the storage level of the corresponding memory cell, for applying a second write voltage to the corresponding memory cell in case that the first data represents the second logic level in order to promote change in the storage level of the corresponding memory cell, for determining whether the corresponding memory cell has reached the second storage level only in case that the first data represents the second logic level and the second data represents the first logic level, for determining whether the corresponding memory cell has reached the third storage level only in case that the first data represents the second logic level and the second data represents the second logic level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the third storage level, and for maintaining the stored first data at the first logic level if the first data storage portion has stored the first date of the first logic level.

159. (New) The device according to claim 158, wherein a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the first logic level is different from a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the second logic level.

160. (New) The device according to claim 158, wherein said first data storage portion includes a CMOS flip-flop circuit, and said second data storage portion includes a CMOS flip-flop circuit.

Cont A10

161. (New) The device according to claim 158, further comprising data detectors for detecting whether all of said first data storage portions have stored the first data of the first logic level.

162. (New) The device according to claim 158, wherein plural of the memory cells store three-bit data.

163. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells, each being capable of having one of first, second and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circus is capable of storing in a data storage portion data of one of first, second, and third logic levels which define write voltage to be applied to a corresponding memory cell, for applying said write voltages to the corresponding memory cell according to the data stored in the data storage portion, for determining whether the corresponding memory cell has reached the second storage level in case that the data stored in the data storage portion represents the second logic level, for determining whether the corresponding memory cell has reached the third storage level in case that the data stored in the data storage portion represents the third logic level, for modifying the stored data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored data from the third logic level to the first logic level if it has been

determined that the corresponding memory cell has reached the third storage level, and for maintaining the data at the first logic level if the data storage portion has stored the data at the first logic level, and

Cont A10

wherein the programming control circuits storing said data of said second logic level determine only whether the corresponding memory cell has reached the second storage level and the programming control circuits storing said data of said third logic level determine only whether the corresponding memory cell has reached the third storage level.

164. (New) The device according to claim 163, wherein said programming control circuits storing the data of the first logic level apply a first write voltage which inhibits changes in the storage levels to the corresponding memory cells.

165. (New) The device according to claim 164, wherein said programming control circuits storing the data of the second logic level apply a second write voltage which promotes changes to the second storage level in the corresponding memory cells, to the corresponding memory cells, and said programming control circuits storing the data of the third logic level apply third write voltage which promotes changes to the third storage level in the corresponding memory cells, to the corresponding memory cells.

166. (New) The device according to claim 165, wherein said second write voltage is different from said third write voltage.

167. (New) The device according to claim 163, wherein each data storage portion includes two CMOS flip-flop circuits.

168. (New) The device according to claim 163, further comprising data detectors for detecting whether all of said data storage portions have stored the data of the first logic level.

169. (New) The device according to claim 163, wherein a couple of the memory cells stores three-bit data.

Cont A10

170. (New) A multi-level non-volatile semiconductor memory device comprising:

a plurality of memory cells, each being capable of having one of first, second and third storage levels; and

a plurality of programming control circuits coupled to each of the memory cells,

wherein each of said programming control circuits is capable of storing in a first data storage portion first data of one of first and second logic levels and of storing in a second data storage portion second data of one of first and second logic levels, for applying first write voltage to a corresponding memory cell in case that the first data represents the first logic level in order to inhibit change in the storage level of the corresponding memory cell, for applying second write voltage to the corresponding memory cell in case that the first data represents the second logic level in order to promote change in the storage level of the corresponding memory cell, for determining whether the corresponding memory cell has reached the second storage level in case that the first data represents the second logic level and the second data represents the first logic level, for determining whether the corresponding memory cell has reached the third storage level in case that the first data represents the second logic level and the second data represent the second logic level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the second storage level, for modifying the stored first data from the second logic level to the first logic level if it has been determined that the corresponding memory cell has reached the third storage level, and for maintaining the stored

first data at the first logic level if the first data storage portion has stored the first data of the first logic level, and

wherein the programming control circuits storing the first data of the second logic level and the second data of the first logic level determine only whether the corresponding memory cell has reached the second storage level, and the programming control circuits storing the first data of the second logic level and the second data of the second logic level determine only whether the corresponding memory cell has reached the third storage level.

171. (New) The device according to claim 170, wherein a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the first logic level is different from a voltage level of the second write voltage to be applied to the memory cell corresponding to the programming control circuit storing the second data of the second logic level.

172. (New) The Device according to claim 170, wherein said first data storage portion includes a CMOS flip-flop circuit, and said second data storage portion includes a CMOS flip-flop circuit.

173. (New) The device according to claim 170, further comprising data detectors for detecting whether all of said first data storage portions have stored the first data of the first logic level.

174. (New) The device according to claim 170, wherein a plural of the memory cells stores three-bit data.--